SHRI VENKATESHWARA UNIVERSITY

Syllabus

M.TECH (VLSI)

(Two Years Post Graduation Programme)

II SEMESTER
(w.e.f. 2019-20)

SCHOOL OF ENGINEERING & TECHNOLOGY

SEMESTER-II													
Sl. No.	**Subject Codes**	**Subject**	**Periods**			**Evaluation Scheme**				**End Semester**		Total	Credit
			L	T	P	CT	TA	Total	PS	TE	PE		
1	MVI-201	Analog and Digital CMOS VLSI Design	3	0	0	20	10	30		70		100	3
2	MVI-202	VLSI Design Verification and Testing	3	0	0	20	10	30		70		100	3
3	MVI-033	Low power VLSI Design	3	0	0	20	10	30		70		100	3
4	MVI-042	Network Security and Cryptography	3	0	0	20	10	30		70		100	3
5	MVI-211	Analog and Digital CMOS VLSI Design Lab	0	0	4				25		25	50	2
6	MVI-212	VLSI Design Verification and Testing Lab	0	0	4				25		25	50	2
7	MVI-221	Mini Project	0	0	4				50		50	100	2
8	AUD-102	DISASTER MANAGEMENT	0	0	0	20	10	30		70		100	0
		Total										700	18

Code	Course Name	L-T-P	Cr.
WVI-201	Analog and Digital CMOS VLSI Design	3-0-0	3

Course Outcomes: At the end of this course, students will be able to

- Analyze, design, optimize and simulate analog and digital circuits using CMOS constrained by the design metrics.
- Connect the individual gates to form the building blocks of a system.
- Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice.

Syllabus Contents:

Technology Scaling and Road map, Scaling issues, Standard 4 mask NMOS Fabrication process

Digital CMOS Design:

Unit 1: Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout,Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noisemargin concepts and their evaluation, Dynamic behavior, Power consumption.

Unit 2: Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model. Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

Unit 3: Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit.Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc.

Analog CMOS Design:

Unit 4: Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common- gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbertcell.

Unit 5: Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise.

Unit 6: Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP, Other compensation techniques.

References:

- J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
- Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition.
- BehzadRazavi , "Design of Analog CMOS Integrated Circuits", TMH, 2007.
- Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition.
- R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008.
- Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design",TMH, 3rdEdition.
- Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition.

Code	Course Name	L-T-P	Cr.
WVI-211	Analog and Digital CMOS VLSI Design Lab	0-0-4	2

Course Outcomes: At the end of the laboratory work, students will be able to:

- Design digital and analog Circuit using CMOS.
- Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice

List of Experiments:

1) Use VDD=1.8V for 0.18um CMOS process, VDD=1.3V for 0.13um CMOS Processand VDD=1V for 0.09um CMOS Process.

a) Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
b) Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt.
c) Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.
d) Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
e) Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS =30mV.

To extract Vth use the following procedure.

I. Plot gm vs VGS using NGSPICE and obtain peak gm point.

II. Plot y=ID/(gm)1/2 as a function of VGS using Ngspice.

III. Use Ngspice to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.

f) Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC loadline and calculate gm, gds, gm/gds, and unity gain frequency.

Tabulate your result according to technologies and comment on it.

2) Use VDD=1.8V for 0.18um CMOS process, VDD=1.2V for 0.13um CMOS Processand VDD=1V for 0.09um CMOS Process.

a) Perform the following

I. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.

II. Plot VTC for CMOS inverter with varying VDD.

III. Plot VTC for CMOS inverter with varying device ratio.

b) b) Perform transient analysis of CMOS inverter with no load and with loadand determine tpHL, tpLH, 20%-to-80% tr and 80%-to-20% tf. (use VPULSE = 2V, Cload = 50fF).

c) Perform AC analysis of CMOS inverter with fanout 0 and fanout 1. (Use Cin= 0.012pF, Cload = 4pF, Rload = k)

3) 3) Use Ngspice to build a three stage and five stage ring oscillator circuit in 0.18um and 0.13um technology and compare its frequencies and time period.

4) Perform the following

a) Draw small signal voltage gain of the minimum-size inverter in 0.18um and 0.13um technology as a function of input DC voltage. Determine the small signal voltage gain at the switching point using Ngspice and compare the values for 0.18um and 0.13um process.

b) Consider a simple CS amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 0.18um technology. (W/L)MN=5, (W/L)MP=10 and L=0.5um for both transistors.

I. Establish a test bench, as explained in the lecture, to achieve VDSQ=VDD/2.

II. Calculate input bias voltage if bias current=50uA.

III. Use Ngspice and obtain the bias current. Compare its value with 50uA.

IV. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in Ngspice (consider 30fF load capacitance).

V. Plot step response of the amplifier for input pulse amplitude of 0.1V. Derive time constant of the output and compare it with the time constantresulted from -3dB BW

VI. Use Ngspice to determine input voltage range of the amplifier

5) Three OPAMP INA. Vdd=1.8V Vss=0V, CAD tool: Mentor Graphics DA. Note: Adjust accuracy options of the simulator (setup->options in GUI). Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.

I. Draw the schematic of op-amp macro model.

II. Draw the schematic of INA.

III. Obtain parameters of the op-amp macro model such that

a. low-frequency voltage gain = 5x104,
b. unity gain BW (fu) = 500KHz,
c. input capacitance=0.2pF,
d. output resistance = ,
e. CMRR=120dB

IV. Draw schematic diagram of CMRR simulation setup.
V. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).
VI. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explainhow CMRR of OPAMP changes with resistor mismatches.
VII. Repeat (iii) to (vi) by considering CMRR of all OPAMPs to be 90dB.

6) Technology: UMC 0.18um, VDD=1.8V. Use MAGIC or Microwind.

a) Draw layout of a minimum size inverter in UMC 0.18um technology using MAGIC Station layout editor. Use that inverter as a cell and lay out three cascaded minimumsized inverters. Use M1 as interconnect line between inverters.
b) Run DRC, LVS and RC extraction. Make sure there is no DRC error. Extract the netlist.
c) Use extracted netlist and obtain tPHLtPLH for the middle inverter using Eldo.
d) Use interconnect length obtained and connect the second and third inverter. Extract the new netlist and obtain tPHL and tPLH of the middleinverter. Compare new values of delay times with corresponding valuesobtained in part 'c'.

Code	Course Name	L-T-P	Cr.
WVI-023	Low power VLSI Design	3-0-0	3

Course Outcomes: At the end of the course, students will be able to:

- CO1: Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.
- CO2: Characterize and model power consumption & understand the basic analysis methods.
- CO3: Understand leakage sources and reduction techniques.

Syllabus Contents:

Unit 1: Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches,dynamic

dissipation in CMOS, effects of Vdd & Vt on speed, constraints on Vt reduction,transistor sizing & optimal gate oxide thickness, impact of technology scaling,technology innovations.
Unit 2: Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

Unit 3: Low Power Clock Distribution: Power dissipation in clock distribution, single driver versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. tolerable skew, chip & package co-design of clock network.

Unit 4: Logic Synthesis for Low Power estimation techniques: Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers.

Unit 5: Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits.

Unit 6: Low Power Microprocessor Design System: power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.

References:

- P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer Academic, 2002
- Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wileysons Inc.,2000.
- J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 1999.
- A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer, 1995.

Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.

Code	Course Name	L-T-P	Cr.
WVI-401	VLSI Design Verification and Testing	3-0-0	3

Course Outcomes: At the end of this course, students will be able to

- Familiarity of Front end design and verification techniques and createreusable test environments.
- Verify increasingly complex designs more efficiently and effectively.
- Use EDA tools like Cadence, Mentor Graphics.

Syllabus Contents:

Unit 1: Verification guidelines: Verification Process, Basic Testbench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Testbench components, Layered testbench, Building layered testbench, Simulation environment phases, Maximum code reuse, Testbench performance.

Unit 2: Data types: Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative arrays, Linked lists, Array methods, Choosing a storage type, Creating new types with typedef , Creating user-defined structures, Type conversion, Enumerated types, Constants strings, Expression width.

Unit 3: Procedural statements and routines: Procedural statements, tasks, functions and void functions, Routine arguments, Returning from a routine, Local data storage, Time values Connecting the testbench and design: Separating the testbench and design, Interface constructs, Stimulus timing, Interface driving and sampling, Connecting it all together, Top-level scope Program – Module interactions.

Unit 4: SystemVerilog Assertions: Basic OOP: Introduction, think of nouns, Not verbs, your first class, where to define a class, OOP terminology, Creating new objects, Object deallocation, Using objects, Static variables vs. Global variables, Class methods, Definingmethods outside of the class, Scoping rules, Using one class inside another, Understanding dynamic objects, Copying objects, Public vs. Local, Straying off course building a testbench.

Unit 5: Randomization: Introduction, What to randomize, Randomization in SystemVerilog, Constraint details solution probabilities, Controlling multiple constraint blocks, Valid constraints, In-line constraints, The pre_randomize and post_randomize functions,

Unit 6: Random number functions, Constraints tips and techniques, Common randomization problems, Iterative and array constraints, Atomic stimulus generationvs. Scenario generation, Random control, Random number generators, Random device configuration.

References:

- Chris Spears, " System Verilog for Verification", Springer, 2nd Edition
- M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers
- IEEE 1800-2009 standard (IEEE Standard for System Verilog— UnifiedHardware Design, Specification, and Verification Language).
- System Verilog website – www.systemverilog.org
- http://www.sunburstdesign.com/papers/CummingsSNUG2006Boston_SystemVerilogEvents.pdf
- General reuse information and resources www.design-reuse.com
- OVM, UVM(on top of SV) www.verificationacademy.com
- Verification IP resources http://www.cadence.com/products/fv/verification_ip/pages/default.aspx
- http://www.synopsys.com/Tools/Verification/FunctionalVerification/VerificationIP/Pages/default.aspx

Code	Course Name	L-T-P	Cr.
WVI-411	VLSI Design Verification and Testing Lab	0-0-4	2

Course Outcomes: At the end of the laboratory work, students will be able to:

- Verify increasingly complex designs more efficiently and effectively.
- Use EDA tools like Cadence, Mentor Graphics.

List of Assignments:

1. Sparse memory
2. Semaphore
3. Mail box
4. Classes
5. Polymorphism
6. Coverage
7. Assertions

Code	Course Name	L-T-P	Cr.
WVI-042	Network Security and Cryptography	3-0-0	3

Course Outcomes: At the end of the course, students will be able to:

- Identify and utilize different forms of cryptography techniques.
- Incorporate authentication and security in the network applications.
- Distinguish among different types of threats to the system and handle the same.

Syllabus Contents:

Unit 1: Security
- Need, security services, Attacks, OSI Security Architecture, one time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

Unit 2: Number Theory
- Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

Unit 3: Private-Key (Symmetric) Cryptography
- Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

Unit 4: Public-Key (Asymmetric) Cryptography

- RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

Unit 5: Authentication

- IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.

Unit 6: System Security

Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Firewall Design Principles, Trusted Systems.

References:

- William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
- Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2nd Edition
- Christopher M. King, ErtemOsmanoglu, Curtis Dalton, "Security Architecture,Design Deployment and Operations", RSA Pres,
- Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W.Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition
- Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident

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Code	Course Name	L-T-P	Cr.
AUD -102	Disaster Management	2-0-0	0

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- **Course Objectives: -**Students will be able to:
- learn to demonstrate a critical understanding of key concepts in disaster risk reduction and humanitarian response.
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- Critically evaluate disaster risk reduction and humanitarian response policy and practice from multiple perspectives. Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflictsituations.
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- Critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in.
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Unit No.	Heading	Content
1	**Introduction**	Disaster: Definition, Factors And Significance; Difference Between Hazard And Disaster; Natural And Manmade Disasters: Difference, Nature, Types And Magnitude.
2	**Repercussions Of Disasters And Hazards**	Economic Damage, Loss Of Human And Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.
3	**Disaster Prone Areas In India**	Study Of Seismic Zones; Areas Prone To Floods And Droughts, Landslides And Avalanches; Areas Prone To Cyclonic And Coastal Hazards With Special Reference To Tsunami; Post-Disaster Diseases And Epidemics

4	**Disaster Preparedness And Management**	Preparedness: Monitoring Of Phenomena Triggering A Disaster Or Hazard; Evaluation Of Risk: Application Of Remote Sensing, Data From Meteorological And Other Agencies, Media Reports: Governmental And Community Preparedness.
5	**Risk Assessment**	Disaster Risk: Concept And Elements, Disaster Risk Reduction, Global And National Disaster Risk Situation. Techniques Of Risk Assessment, Global Co-Operation In Risk Assessment And Warning, People's Participation In Risk Assessment. Strategies for Survival
6	**Disaster Mitigation**	Meaning, Concept And Strategies Of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation And Non-Structural Mitigation, Programs Of Disaster Mitigation In India.

- **SUGGESTED READINGS:**

- R. Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies"'New Royal book Company.
- Sahni, Pardeep Et.Al. (Eds.)," Disaster Mitigation Experiences And Reflections", PrenticeHall Of India, New Delhi.
- Goel S. L. , Disaster Administration And Management Text And Case Studies" ,Deep&Deep Publication Pvt. Ltd., New Delhi.