SHRI VENKATESHWARA UNIVERSITY

Syllabus

M.TECH (VLSI)

(Two Years Post Graduation Programme)

I SEMESTER

(w.e.f. 2019-20)

SCHOOL OF ENGINEERING & TECHNOLOGY

Evaluation for M.Tech (VLSI)

SEMESTER-I													
Sl. No.	**Subject Codes**	**Subject**	**Periods**			**Evaluation Scheme**				**End Semester**		Total	Credit
			L	T	P	CT	TA	Total	PS	TE	PE		
1	MVI-101	RTL Simulation and Synthesis with PLDs	3	0	0	20	10	30		70		100	3
2	MVI-102	Microcontrollers and Programmable Digital Signal Processors	3	0	0	20	10	30		70		100	3
3	MVI-011	Digital Signal and Image Processing	3	0	0	20	10	30		70		100	3
4	MVI-021	Parallel Processing	3	0	0	20	10	30		70		100	3
5	MVI-111	RTL Simulation and Synthesis with PLDs Lab	0	0	4				25		25	50	2
6	MVI-112	Microcontrollers and Programmable Digital Signal Processors Lab	0	0	4				25		25	50	2
7	MLC-101	Research Methodology and IPR	2	0	0	20	10	30		70		100	2
8	AUD-101	English for Research Paper Writing	2	0	0	20	10	30		70		100	0
		Total										700	18

Code	Course Name	L-T-P	Cr.
WVI-301	RTL Simulation and Synthesis with PLDs	3-0-0	3

Course Outcomes: At the end of the course, students will demonstrate the ability to:

- Familiarity of Finite State Machines, RTL design using reconfigurable logic.
- Design and develop IP cores and Prototypes with performance guarantees
- Use EDA tools like Cadence, Mentor Graphics and Xilinx.

Syllabus Contents:

Unit1: Top down approach to design, Design of FSMs (Synchronous and asynchronous), Static timing analysis, Meta-stability, Clock issues, Need and design strategies for multi- clock domain designs.

Unit 2: Design entry by Verilog/VHDL/FSM, Verilog AMS.

Unit 3: Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA, SoC, Floor planning, Placement, Clock tree synthesis, Routing, Physical verification, Power analysis, ESD protection.

Unit 4: Design for performance, Low power VLSI design techniques. Design for testability.

Unit 5: IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP, Use of external hard IP during prototyping.

Unit 6: Case studies and Speed issues.

References:

- Richard S. Sandige, “Modern Digital Design”, MGH, International Editions.
- Donald D Givone, “Digital principles and Design”, TMH Charles Roth, Jr. and Lizy K John, “Digital System Design using VHDL”, Cengage Learning.
- Samir Palnitkar, “Verilog HDL, a guide to digital design and synthesis”, Prentice Hall.
- Doug Amos, Austin Lesea, Rene Richter, “FPGA based prototyping methodology manual”, Xilinx

- Bob Zeidman, “Designing with FPGAs & CPLDs”, CMP Books.

Code	Course Name	L-T-P	Cr.
WVI-311	RTL Simulation and Synthesis with PLDs Lab	0-0-4	2

Course Outcomes: At the end of the laboratory work, students will be able to:

- Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools.
- Use EDA tools like Cadence, Mentor Graphics and Xilinx.

List of Experiments:

1) Verilog implementation of 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder, D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters, Binary to Gray converter, Parity generator.
2) Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
3) Vending machines - Traffic Light controller, ATM, elevator control.
4) PCI Bus & arbiter and downloading on FPGA.
5) UART/ USART implementation in Verilog.
6) Realization of single port SRAM in Verilog.
7) Verilog implementation of Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier.
8) Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.

Code	Course Name	L-T-P	Cr.
MLC-301	Research Methodology and IPR	2-0-0	2

Course Outcomes: At the end of this course, students will be able to

- Understand research problem formulation.
- Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

Syllabus Contents:

Unit 1: Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations.

Unit 2: Effective literature studies approaches, analysis Plagiarism, Research ethics,

Unit 3: Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

Unit 4: Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Processof Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

Unit 5: Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

Unit 6: New Developments in IPR: Administration of Patent System. New developmentsin IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

References:

- Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
- Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
- Ranjit Kumar, 2nd Edition , "Research Methodology: A Step by Step Guide for beginners"
- Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
- Mayall , "Industrial Design", McGraw Hill, 1992.
- Niebel , "Product Design", McGraw Hill, 1974.
- Asimov , "Introduction to Design", Prentice Hall, 1962.
- Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age", 2016.
- T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

Code	Course Name	L-T-P	Cr.
WVI-031	Parallel Processing	3-0-0	3

Course Outcomes: At the end of this course, students will be able to

- Identify limitations of different architectures of computer
- Analysis quantitatively the performance parameters for different architectures.
- Investigate issues related to compilers and instruction set based on type of architectures.

Syllabus Contents:

Unit 1: Overview of Parallel Processing and Pipelining, Performance analysis,Scalability

Unit 2: Principles and implementation of Pipelining, Classification of pipeliningprocessors, Advanced pipelining techniques, Software pipelining.

Unit 3: VLIW processors
Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC,MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture.

Unit 4: Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions

Unit 5: Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, DataParallel Programming, Parallel Software Issues

Unit 6: Operating systems for multiprocessors systems Customizing applications onparallel processing platforms.

References:

- Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing", MGH International Edition
- Kai Hwang, "Advanced Computer Architecture", TMH
- V. Rajaraman, L. Sivaram Murthy, "Parallel Computers", PHI.
- William Stallings, "Computer Organization and Architecture, Designing for performance" Prentice Hall, Sixth edition
- Kai Hwang, Zhiwei Xu, "Scalable Parallel Computing", MGH
- David Harris and Sarah Harris, "Digital Design and Computer Architecture",Morgan Kaufmann.

Code	Course Name	L-T-P	Cr.
WVI-101	Microcontrollers and Programmable Digital Signal Processors	3-0-0	3

Course Outcomes: At the end of this course, students will be able to

- Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.
- Identify and characterize architecture of Programmable DSP Processors.
- Develop small applications by utilizing the ARM processor core and DSP processor based platform.

Syllabus Contents:

Unit 1: ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces

Unit 2: Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

Unit 3:LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT

Unit 4: Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family.

Unit 5:VLIW architecture and TMS320C6000 series, architecture study, data paths,cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.

Unit 6: Code Composer Studio for application development for digital signal processing,On chip peripherals , Processor benchmarking.

References:

1. Joseph Yiu, “The definitive guide to ARM Cortex-M3”, Elsevier, 2nd Edition.
2. Venkatramani B. and Bhaskar M. “Digital Signal Processors: Architecture, Programming and Applications” , TMH , 2nd Edition
3. Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designing and Optimizing”, Morgan Kaufman Publication

4. Steve furber, “ARM System-on-Chip Architecture”, Pearson Education
5. Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley
6. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com

Code	Course Name	L-T-P	Cr.
WVI-111	Microcontrollers and Programmable Digital Signal Processors Lab	0-0-4	2

Course Outcomes: At the end of the laboratory work, students will be able to:

- Install, configure and utilize tool sets for developing applications based on ARM processor core SoC and DSP processor.
- Develop prototype codes using commonly available on and off chip peripheralson the Cortex M3 and DSP development boards.

List of Assignments:

Part A) Experiments to be carried out on Cortex-M3 development boards and usingGNU tool chain

1. Blink an LED with software delay, delay generated using the SysTick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flashthe LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.

9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.

10. System reset using watchdog timer in case something goes wrong.

11. Sample sound using a microphone and display sound levels on LEDs.

Part B) Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

1. To develop an assembly code and C code to compute Euclidian distance betweenany two Points

2. To develop assembly code and study the impact of parallel, serial and mixed execution

3. To develop assembly and C code for implementation of convolution operation

4. To design and implement filters in C to enhance the features of given input sequence/signal

ELECTIVE-I

Code	Course Name	L-T-P	Cr.
WVI-011	Digital Signal and Image Processing	3-0-0	3

Course Outcomes: At the end of this course, students will be able to

- Analyze discrete-time signals and systems in various domains
- Design and implement filters using fixed point arithmetic targeted for embedded platforms.
- Compare algorithmic and computational complexities in processing and coding digital images.

Syllabus Contents:

Unit 1: Review of Discrete Time signals and systems, Characterization in time and Zand Fourier – domain, Fast Fourier Transform algorithms – In-place computations, Butterfly computations, bit reversal's.

Unit 2: Digital Filter design: FIR - Windowing and Frequency Sampling, IIR – Impulseinvariance, bilinear Transformation.

Unit 3: Fixed point implementation of filters – challenges and techniques.

Unit 4: Digital Image Acquisition, Enhancement Restoration. Digital Image Coding andCompression – JPEG and JPEG 2000.

Unit 5: Color Image processing – Handling multiple planes, computational challenges.

Unit 6: VLSI architectures for implementation of Image Processing algorithms, Pipelining.

References:

- J.G. Proakis, Manolakis "Digital Signal Processing", Pearson, 4th Edition
- Gonzalez and Woods, "Digital Image Processing", PHI, 3rd Edition
- S. K. Mitra. "Digital Signal Processing – A Computer based Approach", TMH, 3rd Edition, 2006
- A. K. Jain, "Fundamentals of Digital Image Processing", Prentice Hall
- KeshabParhi, "VLSI Digital Signal Processing Systems – Design and Implementation", Wiley India

Code	Course Name	L-T-P	Cr.
AUD -101	English for Research Paper Writing	2-0-0	0

Course objectives: Students will be able to:

- Understand that how to improve your writing skills and level of readability
- Learn about what to write in each section
- Understand the skills needed when writing a Title

Syllabus- Content:

Unit No.	Content

1	Planning and Preparation, Word Order, Breaking up long sentences,Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness
2	Clarifying Who Did What, Highlighting Your Findings, Hedging and 4 Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction
3	Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.
4	key skills are needed when writing a Title, key skills are needed whenwriting an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature
5	skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions useful phrases, how to ensure paper is as good as it could possibly be the 4 first- time submission.

Suggested Studies:

Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book .Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011